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10/062,426	02/05/2002	Tae Yamane	OKI.302	4137

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 10/062,426	Applicant(s) YAMANE, TAE	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 02/05/02 is acceptable.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

A. Claims 1, 5, 9, and 12 include the limitations "a metal pad formed on the semiconductor chip" and "a molding resin formed over the conductive wiring pattern" in lines 3 and 7 respectively.

Claim 17, line 3 includes the limitation "a pad which is formed on the semiconductor chip".

Therefore, the metal pad and the molding resin must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

B. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Sp cification

3. The disclosure is objected to because of the following informalities:

Page 8, line 10: Delete "patterns 12" and insert ---" patterns 18"---.

Appropriate correction is required.

Claim Objections

4. Claims 1, 5, 9 and 12 are objected to because of the following informalities:

A. The claim limitation "connecting portion (boundary portion)" as recited in claims 1 and 5, line 12 and claim 9, line 13, should read "connecting portion".

B. The claim limitation "extending vertically" as recited in claim 12, line 14, should read "extending laterally or in a perpendicular direction".

Appropriate correction is required.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 02/05/02 has been considered.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) in view of Takao et al. (Japanese Pat. 2000-183214).

Regarding claim 1, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)
- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60-Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip
- conductive wiring patterns (108B-2/108-3 in Fig. 1A) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, line 1-10)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns

- conductive pads/metal posts (109B in Fig. 1A; Col. 4, line 4) being formed in the molding resin
- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20) being formed connecting the wiring pattern, and
- a connecting portion of the of the wiring patterns and the conductive pad/post being provided with a slit (see slit SB between 108 B1-B3/108Bb and 109B) to disperse/reduce stress and to prevent cracking/destruction and sliding of the wiring patterns/layer (Col. 2, lines 27-40)

(Fig. 1A/1B; Col. 2, line 25- Col. 5, line 22).

Nishimoto fails to explicitly show in a cross-sectional view of Fig. 1A/1B, the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin.

Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation, page 1 of 1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et

al. so that an electrical testing and rework capability can be improved in Nishimoto's CSP.

Regarding claim 2, Nishimoto and Takao et al. teach substantially the entire claimed structure as applied to claim 1 above, and Nishimoto further teaches the connecting portion between the wiring patterns and conductive pad/post (208Aa/208Ab/208A-1 and 209A respectively in Fig. 3) being provided with a plurality of slits separated from each other (see slits S in Fig. 3; Col. 5, lines 22-48).

Regarding claim 3, Nishimoto and Takao et al. teach substantially the entire claimed structure as applied to claims 1 and 2 above, and Nishimoto further teaches the slits having different shapes/arrangements including rectangular shapes and other shapes having end and middle sections (each section not being numerically referenced in Fig. 3, see slits S in Fig. 3), the end sections being parallel to the main wiring pattern (208A-1 in Fig. 3) and the middle sections being extended radially (see slits S in wiring pattern 208A-2 in Fig. 3; Col. 5, lines 22-48).

Regarding claim 12, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)

- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60- Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip
- conductive wiring patterns (108B-1,108B-2, 108-3 and 108Bb in Fig. 1A) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, line 1-10)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns
- conductive pads/metal posts (109B in Fig. 1A; Col. 4, line 4) being formed in the molding resin
- the conductive wiring patterns being shaped/patterned to have a first region (108B-1 and 108B-2 in Fig. 1A) extending outwardly/ in a longitudinal direction from the conductive pads/metal posts and a second region (108Ba, 108Bb, etc. in Fig. 1A) extending in a perpendicular/lateral direction from the first region, and
- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20) being formed connecting the wiring pattern

(Fig. 1A/1B; Col. 2, line 25- Col. 5, line 22).

Nishimoto fails to explicitly show in a cross-sectional view of Fig. 1A/1B, the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin.

Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation, page 1 of 1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et al. so that an electrical testing and rework capability can be improved in Nishimoto's CSP.

Regarding claim 13, Nishimoto and Takao et al. teach substantially the entire claimed structure as applied to claim 12 above, and Nishimoto further teaches the second region comprising a plurality of projecting parts/branched sections (108Ba, 108Bb, etc. in Fig. 1A), each extending in a perpendicular/lateral direction from the first region (Col. 4, line 36-50).

Regarding claim 14, Nishimoto and Takao et al. teach substantially the entire claimed structure as applied to claims 12 and 13 above, and Nishimoto further teaches using a wiring pattern including a first and second regions (104 and 105 respectively in Fig. 1A) where projecting parts/branched sections (see 105 on both sides of wiring 104 in Fig. 1A) of a second region of the wiring pattern are extended from both sides of the first region (Col. 3, line 55- Col. 4, line 20).

8. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) in view of Takao et al. (Japanese Pat. 2000-183214) and Owada et al. (US Pat. 5220199).

Regarding claim 5, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)
- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60- Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip
- conductive wiring patterns (108B-1/108B-2/108-3/108Bb and 208A-1/208A-2 in Fig. 1A and 3 respectively) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, lines 1-10; Col. 5, lines 22-40)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns
- conductive pads/metal posts (109B and 209A in Fig. 1A and 3 respectively; Col. 4, line 4; Col. 5, line 28) being formed in the molding resin, and
- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20; Col. 5, line 29) being formed connecting the wiring pattern

(Fig. 1A/1B and 3; Col. 2, line 25- Col. 5, lines 22-48).

Nishimoto fails to:

a) explicitly show in a cross-sectional view of Fig. 1A/1B, the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin, and

b) a dummy pattern arranged adjacent a connecting portion of the conductive post and the wiring pattern.

a) Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation, page 1 of 1).

b) Owada et al. teach arranging dummy patterns (8 in Fig. 7) adjacent/proximity of a connecting portion of a third level wiring (7a in Fig. 7 and 4) and a conductive plug/post (see metallization in through-hole 28 connecting wirings 25a and 7a in Fig. 4/7) to minimize an increase in the parasitic capacitance in a multilayered wiring structure (Col. 9, line 25 and Col. 5, line 46).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et al. and a dummy pattern being arranged adjacent a connecting portion of the conductive post and the wiring pattern as taught by Owada et al. so that an increase in the parasitic

capacitance can be minimized and an electrical testing and rework capability can be improved in Nishimoto's CSP.

Regarding claim 6, Nishimoto, Takao et al. and Owada et al. teach substantially the entire claimed structure as applied to claim 5 above, except the dummy pattern being formed in the same process as that of the conductive pattern and being arranged parallel to the conductive pattern.

Owada et al. further teach forming the dummy pattern in a striped/bar-like parallel arrangement with respect to the wiring lines of the conductive pattern (7b and 8 in Fig. 3) where the dummy pattern is formed in the same process/fabrication step and with the same material as that of the conductive pattern (Col. 5, line 35).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dummy pattern being formed in the same process as that of the conductive pattern and being arranged parallel to the conductive pattern as taught by Owada et al. so that the process cycle time and an electrical testing/rework capability can be improved and an increase in the parasitic capacitance can be minimized in Takao et al. and Nishimoto's CSP.

Regarding claim 7, Nishimoto, Takao et al. and Owada et al. teach substantially the entire claimed structure as applied to claim 5 above, except the dummy pattern comprising two parts being arranged at both sides of the conductive pattern.

Owada et al. further teach forming the dummy patterns in a mesh-like arrangement having two or more parts/portions along/on both sides of the conductive wiring (see 8 and 7b in Fig. 7 and 3).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dummy pattern comprising two parts being arranged at/along both sides of the conductive pattern as taught by Owada et al. so that planarization of the insulating layers and an electrical testing/rework capability can be improved and an increase in the parasitic capacitance can be minimized in Takao et al. and Nishimoto's CSP.

9. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) in view of Takao et al. (Japanese Pat. 2000-183214) and Bertolet et al. (US Pat. 5844317).

Regarding claim 9, Nishimoto discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (101 in Fig. 1A/1B)
- electrodes/regions having gate and source/drain connections being formed on the chip (see connecting portions C1/104, C2 and C3 Fig. 1A; Col. 3, line 60-Col. 4, line 10)
- an insulating film/wafer coat (107 in Fig. 1A/1B) formed over the chip

- conductive wiring patterns (108B-1/108B-2/108-3/108Bb and 208A-1/208A-2 in Fig. 1A and 3 respectively) being formed on the insulating film/wafer coat, the metal electrode/pad being electrically connected to the wiring pattern (Col. 4, lines 1-10; Col. 5, lines 22-40)
- a molding resin (111 in Fig. 1B) being formed over the conductive wiring patterns
- conductive pads/metal posts (109B and 209A in Fig. 1A and 3 respectively; Col. 4, line 4; Col. 5, line 28) being formed in the molding resin, and
- terminals such as ground, power, etc. (not numerically referenced in Fig. 1A; Col. 4, line 20; Col. 5, line 29) being formed connecting the wiring pattern

(Fig. 1A/1B and 3; Col. 2, line 25- Col. 5, lines 22-48).

Nishimoto further discloses using recesses/dents in the conducting wiring pattern to provide the thinning of the wiring pattern (Col. 5, line 61).

Nishimoto fails to:

a) explicitly show in a cross-sectional view of Fig. 1A/1B, the metal pad on the chip and the conductive post in the resin being connected with the terminal formed on the molding resin, and

b) at least one of the conducting wiring pattern and conductive post is provided with a dent around a connecting portion of the conducting wiring pattern and conductive post.

a) Takao et al. teach a conventional CSP having a chip with a metal/aluminum pad (52 in Fig. 11) where a conductive post (55 in Fig. 11) formed in a resin (54 in Fig. 11) is connected to a terminal/bump (56 in Fig.11) on the resin (see Prior art description in English Translation).

b) Bertolet et al. teach using a recess/dent (30 in Fig. 1 and 2) around a connecting portion of the conducting wiring pattern and conductive post (16 and 20 respectively in Fig. 1 and 2; Col. 7, line 25- Col. 8, line 42).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the conductive post being formed in the resin and the terminal being formed on the molding resin being connected as taught by Takao et al. and at least one of the conducting wiring pattern and conductive post is provided with a dent around a connecting portion of the conducting wiring pattern and conductive post as taught by Bertolet et al. so that the cracking/delamination defects in the wiring layer can be reduced and the insulation coverage of the wiring layer and an electrical testing/rework capability can be improved in Nishimoto's CSP.

Regarding claim 10, Nishimoto, Takao et al. and Bertolet et al. teach substantially the entire claimed structure as applied to claim 9 above, except the dent being shaped to be a square.

Bertolet et al. further teach the recess having length/width dimensions being such that the recess/dent has a rectangular shape (30 in Fig. 1) or selecting the width being higher or lower such that the recess/dent can be formed having a square or a rectangular shape (Col. 8, lines 27-33).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dent being shaped to be a square as taught by Bertolet et al. so that the insulation coverage of the wiring layer can be improved and the photo/etch processing can be simplified in Nishimoto's CSP.

10. Claims 4, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036) and Takao et al. (Japanese Pat. 2000-183214), as applied to claims 1 and 12 above, and further in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 4, Nishimoto and Takao et al. teach substantially the entire claimed structure as applied to claim 1 above, except the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that an area of the connecting portion gradually decreases from a circular conductive pad/post portion of the wiring pattern (21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Takao et al. and Nishimoto's CSP.

Regarding claim 15, Nishimoto and Takao et al. teach substantially the entire claimed structure as applied to claim 12 above, except the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that an area of the connecting portion gradually decreases from a circular conductive pad/post portion of the wiring pattern (21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Takao et al. and Nishimoto's CSP.

Regarding claim 16, Nishimoto and Takao et al. and Ogawa et al. teach substantially the entire claimed structure as applied to claims 12 and 15 above, and Nishimoto further teaches a projecting part/branched section (108B1 in Fig. 1A) of the conductive wiring pattern (108B-2 in Fig. 1A) being a part of the conductive pad/metal post (109B in Fig. 1A; Col. 4, lines 1-50).

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036), Takao et al. (Japanese Pat. 2000-183214) and Owada et al. (US Pat. 5220199), as applied to claims 1 and 7 above, and further in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 8, Nishimoto, Takao et al. and Owada et al. teach substantially the entire claimed structure as applied to claims 5 and 7 above, except the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that an area of the connecting portion gradually decreases from a circular conductive pad/post portion of the wiring pattern (21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Owada et al., Takao et al. and Nishimoto's CSP.

12. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto (US Pat. 5289036), Takao et al. (Japanese Pat. 2000-183214) and Bertolet et al. (US Pat. 5844317), as applied to claim 9 above, and further in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 11 Nishimoto, Takao et al. and Bertolet et al. teach substantially the entire claimed structure as applied to claim 10 above, except the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape such that an area of the connecting portion gradually decreases from a circular conductive pad/post portion of the wiring pattern (21a/21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to a narrow/linear portion of the conductive wiring pattern (21 in Fig. 2B; Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the connecting portion being shaped to decrease in area gradually from the conductive post to the conductive wiring as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Bertolet et al., Takao et al and Nishimoto's CSP.

13. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (Japanese Pat. 2000-183214) in view of Ogawa et al. (US Pat. 6237218).

Regarding claim 17, Takao et al. disclose a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (51 in Drawing 11)
- a pad /electrode (52 in Drawing 11) being formed on the chip
- a composite insulating film having a lower and upper layers (54 in Drawing 11, lower layer not numerically referenced in Drawing) being formed over the chip
- a conductive portion/wiring layer (53 in Drawing 11) being electrically connected to the pad/electrode
- the conductive portion comprising:

  a) first portion being formed on the lower insulating film and the pad (not numerically referenced in Drawing 11, see portion of 53 above the pad 52 in Drawing 11), and

- b) a second portion having a connection/contacting part contacting the first portion (not numerically referenced in Drawing 11, see portion of 53 under bump 56 in Drawing 11)

(Drawing 11; Prior art description in English Translation, page 1of 1).

Takao et al. fail to teach the contacting part connecting the first and second portions of the conductive portion being gradually narrow toward the first portion.

Ogawa et al. teach using a wiring substrate having a conductive wiring pattern/shape on the insulating layer (21 and 22b/22c respectively in Fig. 1 and 2B), the conductive wiring having a first/narrow portion and a second/wide portion (each portion not numerically referenced in Fig. 11, see linear portion and circular/pad portion of wiring 21 respectively in Fig. 2B) such that an area/width of a connecting part between the two sections gradually decreases from a center of the second portion (21b/21c/21d and respective wiring layer 21 in Fig. 2B and 1) to the first portion (Col. 12, line 55- Col. 13, line 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the contacting part being shaped to be gradually narrow toward the first conductive portion as taught by Ogawa et al. so that the insulation cracking and stress related defects can be reduced in Takao et al's CSP.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References E and O are cited as being related to CSP having stress reducing metallization structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
06-26-03

Nitin Parekh

PATENT EXAMINER
TECHNOLOGY CENTER 2800